ABSTRACT

A direct calibration technique significantly tightens a tolerance band between multiple voltage controlled oscillators (VCOs), to correct for slight frequency mismatch between the multiple VCOs. The tightened tolerance band enhances the bit error rate (BER) and/or lengthens the possible consecutive identical digits (CIDs) length, and is particularly useful in integrated circuit applications. A Frequency Locked Loop (FLL), an accumulator, and a DAC are implemented to form a calibration loop that becomes far more digital in nature than a PLL, permitting greater embedded circuit test coverage and ease of integration in VLSI digital technologies. A frequency calibrated loop with digital accumulator and DAC in lieu of a PLL with associated charge pump integrator eliminates the need for large integrated capacitors, sensitivity to drift due to the leakage currents associated with deep sub-micron technologies, and embedded analog voltages which generally cannot be tested.